Docket No.: 50432-477 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
William G. EN, et al.	:	Confirmation Number: 20277
Serial No.: 10/021,497	:	Group Art Unit: 2822
Filed: December 19, 2001	:	Examiner: IDA M. SOWARD

For: ARRAY OF GATE DIELECTRIC STRUCTURES TO MEASURE GATE DIELECTRIC THICKNESS AND PARASITIC CAPACITANCE

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed December 17, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1-6, 8, and 10-23 are pending in this application. Claims 11-20 are withdrawn from

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consideration pursuant to a restriction requirement. Claims 1-6, 8, and 21-23 have been finally rejected. It is from the final rejection of claims 1-6, 8, and 21-23 that this appeal is taken.

IV. STATUS OF AMENDMENTS

No amendment has been filed subsequent to the imposition of the final Office Action dated October 21, 2003.

V. SUMMARY OF INVENTION

This invention addresses and solves the problem of accurately measuring the gate dielectric thickness and the capacitance of gate dielectric capacitors (page 2, lines 18 to 23 of the written description). This invention provides a wafer comprising a plurality of dummy structures that allows gate dielectric thickness and capacitance to be monitored and measured with improved accuracy before the wafer is cut into individual chips (page 6, lines 8 and 9 of the written description).

An important aim of ongoing research in the semiconductor industry is the reduction in the dimensions of semiconductor devices. As the size of planar transistors such as metal oxide semiconductor field effect transistors (MOSFET) devices decreases, the dimensions of the gate electrodes and gate dielectric layers decrease correspondingly. Tight control of the gate dielectric thickness is necessary to manufacture reduced-size, high-reliability, high-speed transistors. If the gate dielectric thickness is too thin, short-circuiting is a problem. If the gate dielectric layer is too thick, then the device speed will be too slow (page 1, lines 5 to 18 of the written description).

The thickness of the gate dielectric layer can be determined by measuring the capacitance of the

gate dielectric capacitor. The thickness of the gate dielectric layer is related to the capacitance by the following formula:

$$t = k/C$$

wherein t is the thickness of the gate dielectric layer, k is the dielectric constant of the gate dielectric layer, and C is the capacitance of the gate dielectric capacitor (page 1, lines 19 to 24 of the written description).

However, the capacitance of large area, ultra-thin gate dielectric capacitors and small area gate dielectric capacitors cannot be accurately measured directly. The large area gate dielectric capacitors tend to suffer from high gate leakage through the gate. Gate leakage does not appreciably hinder measuring the capacitance of small area gate dielectric capacitors, rather parasitic capacitance interferes with accurate gate dielectric capacitance measurements in small area gate dielectric capacitors. As the area of the gate dielectric capacitor is reduced, the proportion of the total capacitance due to the parasitic capacitance associated with the wiring structures increases (page 2, lines 1 to 8 of the written description).

Accurate measurement of the gate dielectric thickness and the capacitance of gate dielectric capacitors can be achieved with embodiments of the present invention, which provide a wafer comprising a base layer and an active layer formed on the base layer. A gate dielectric layer is formed on the active layer and a conductive layer is formed on the gate dielectric layer. A plurality of isolation regions are formed in the wafer and the wafer is divided into a plurality of first portions, second portions, and third portions. The first portions comprise gate dielectric capacitors, wherein the gate dielectric capacitors comprise a first electrode layer formed from the active layer, an insulating layer formed from the gate dielectric layer, and a second electrode layer formed from the conductive layer.

The second portions comprise first dummy structures, wherein the first dummy structures comprise a first electrode layer formed from the active layer and an insulating layer formed from the gate dielectric layer. The third portions comprise second dummy structures, wherein the second dummy structures comprise an insulating layer formed from an isolation region and a second electrode layer formed from the conductive layer. The third portion does not contain the active layer (page 2, line 23 to page 3, line 3; and page 15, lines 15 to 19 of the written description.)

This invention addresses the needs for an improved method of measuring the capacitance and gate dielectric thickness of ultra-thin gate dielectric capacitors. The present invention eliminates parasitic capacitance from the gate dielectric capacitance measurements enabling accurate measurement of the gate dielectric capacitor capacitance.

VI. ISSUES

A. The Rejection

Claims 1-6, 8, 10, and 21-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Admitted Prior Art (APA) (Figure 7) in view of Tuan et al. (U.S. Pat. App. 2002/0151141) and Baliga (U.S. Pat. App. 2002/0177277).

B. The Issues

The Issues that arise in this appeal that require resolution by the Honorable Board of Appeals and Interferences (the Board) are:

Whether claims 1-6, 8, 10, and 21-23 are unpatentable under 35 U.S.C. § 103(a) for obviousness as predicated upon the combination of APA, Tuan et al., and Baliga.

VII. GROUPING OF CLAIMS

There are three groups of claims. Claims 1-6, 8, 10, and 22 all stand or fall together. Claims 21 and 23 stand separately. Separate arguments in support of each group are presented *infra.*

VIII. THE ARGUMENT

A. The Examiner's Position

The Examiner asserted that Prior Art Figure 7 of the instant specification teaches a wafer comprising a base layer, gate dielectric layer, conductive layer, active region, a plurality of shallow isolation regions, and a metal interconnect. The Examiner acknowledged that the admitted prior art does not teach a wafer divided into a plurality of the claimed first, second, and third portions. The Examiner relied on Tuan et al. to provide a teaching of a wafer divided into first, second, and third portions, wherein the first portion comprises a gate electrode and the third portion comprises a second dummy structure. The Examiner further relied on Baliga to provide a teaching of the second portion (first dummy structure). The Examiner averred that the Tuan et al. dummy structures 141 correspond to the claimed second dummy structure and that the Baliga dummy structure 118c corresponds to the claimed first dummy structure. The Examiner concluded that it would have been obvious to modify the Admitted Prior Art gate structure to include the dummy structures of Tuan et al. and Baliga to provide a structure that can support high voltages.

B. Appellants' Position

The Admitted Prior Art, Tuan et al., and Baliga, whether taken alone, or in combination, do not suggest the claimed wafer. The Examiner proposed combination does not disclose or suggest the first

dummy structure. There is no motivation to include a selected portion of the Baliga structure in the Admitted Prior Art to obtain the device of claims 1, 21, and 23.

Claims 1, 21, and 23 require that the second portion does not contain the conductive layer. The Examiner asserted that the dummy structure 118c of Baliga comprises the first electrode layer and an insulating layer. The Examiner asserted that the doped silicon active layer of Baliga corresponds to the first electrode layer and that the insulating layer of Baliga corresponds to the gate dielectric layer.

The Examiner asserted that incorporating the second portions of Baliga into the APA would provide a structure that can support high voltages. However, the Examiner does not include the required conductive layers 118a, 118b, 118c of the Baliga structure when combining Baliga with the APA. Layers 118a, 118b, and 118c of Baliga are formed from the same layer and correspond to the conductive layer (second electrode layer) of a gate capacitor. The Examiner apparently ignored the Baliga conductive layers 118a, 118b, and 118c that are required components of the Baliga device. It is not seen how it is possible for the Examiner to allege motivation to only include a part of the asserted Baliga second portion in the APA. Presumably, the motivation asserted to be taught by Baliga would require the substitution of the entire asserted second portion. The entire asserted second portion of Baliga would include the conductive layers 118a, 118b, and 118c. However, claims 1, 21, and 23 explicitly exclude the presence of the conductive layers in the claimed second portions. Therefore, the combination of Baliga with Tuan et al. and the APA would not provide nor suggest the claimed wafer.

Claim 21 is further distinguishable because claim 21 requires that the active layer comprises source/drain regions. The Examiner asserted active layer 124 of Tuan et al. does not comprise source/drain regions. In addition, there is no motivation in Baliga to substitute source and drain regions into the first electrode layer 124 of Tuan et al.

Claim 23 is further distinguishable over the cited prior art because the cited prior art does not

suggest the claimed wafer wherein the gate dielectric layer is located between the first electrode layer and the second electrode layer. For example, the gate dielectric layer 108 of Tuan et al. is located beneath the Examiner asserted first and second electrode layers 124, 128, not between the electrode layers, as required by claim 23.

There is no suggestion in the cited references to combine Tuan et al., Baliga, and the APA as asserted by the Examiner to provide the claimed wafer.

The dummy gate structures of Tuan et al. protect circuit elements during chemical-mechanical polishing (CMP). The APA does not disclose performing CMP after forming circuit elements, as taught by Tuan et al. Therefore, there would be no suggestion to include the dummy structures of Tuan et al. in the wafer of the APA. Furthermore, Tuan et al. teach a high voltage portion 4402 of the semiconductor structure. Because the semiconductor structure of Tuan et al. already supports high voltage, there is no motivation to include the additional dummy structures of Baliga. One of ordinary skill in this art would not be motivated to include additional dummy structures to provide a structure that can support high voltages, when the structure already can support high voltages without the additional dummy structures.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge readily available to one of ordinary skill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). There is no suggestion in Tuan et al. or Baliga of substituting the claimed first and second dummy structures into the wafer of the Admitted Prior Art. There is no suggestion in Tuan et al. or Baliga of forming the claimed second portion in the wafer of the APA, as

required by claims 1, 21, and 23. There is no suggestion in Tuan et al. or Baliga to form the active layer comprising source/drain regions, as required by claim 21. In addition, there is no suggestion in Tuan et al. or Baliga to form the gate dielectric layer between the first and second electrode layers, as required by claim 23.

The mere fact that references can be modified does not render the resulting combination obvious unless the prior art also suggests the desirability of the modification. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Tuan et al. and Baliga do not suggest the desirability of forming the claimed first and second dummy structures and a gate dielectric capacitor on a wafer, as required by the instant claims.

The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103 is not an abstract concept, but must stem from the applied prior art as a whole and realistically impel one having ordinary skill in the art to modify a specific reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Accordingly, the Examiner is charged with the initial burden of identifying a source in the applied prior art for the requisite realistic motivation. *Smiths Industries Medical System v. Vital Signs, Inc.,* 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999); *In re Mayne*, 104 F.3d 1339, 41 USPQ2d 1449 (Fed. Cir. 1997). There is no motivation in Tuan et al. or Baliga to form a wafer comprising the claimed first and second dummy structures and a gate dielectric capacitor.

The only teaching of the claimed wafer comprising a plurality of first portions, second portions comprising a first dummy structure, and third portions comprising a second dummy structure is found in Appellants' disclosure. However, the teaching or suggestion to make a claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on appellants'

disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Examiner's conclusion of obviousness is not supported by any factual evidence. The Examiner has not provided a factual basis for asserting that the combination of the Admitted Prior Art, Tuan et al., and Baliga would provide the claimed invention. The Examiner's retrospective assessment of the claimed invention and use of unsupported conclusory statements are not legally sufficient to generate a case of *prima facie* obviousness. The motivation for modifying the prior art must come from the prior art and must be based on facts.

The Examiner asserted that motivation for combining the references can be found in paragraph 013 of Tuan et al. However, no discernible motivation is found in Tuan et al. Perhaps, the Examiner intended to refer to paragraph 013 of Baliga. As explained above, it is not seen how Baliga can provide the asserted motivation when the Examiner selectively omits critical portions of the Baliga device from the asserted combination.

IX. CONCLUSION

Based upon the arguments submitted supra, Appellants respectfully submit that the Examiner's rejections under 35 U.S.C. § 103 are not legally viable. Appellants, therefore, respectfully solicit the Honorable Board to reverse the Examiner's rejections of claims 1-6, 8, 10, and 21-23 as obvious as evidenced by the APA, Tuan et al., and Bilaga.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Bernard P. Codd
Registration No. 46,429

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 BPC:rrh
Date: February 13, 2004
Facsimile: (202) 756-8087

X. APPENDIX

APPEALED CLAIMS:

1. A wafer comprising:

a base layer;

an active layer formed on the base layer;

a gate dielectric layer formed on the active layer;

a conductive layer formed on the gate dielectric layer; and

a plurality of isolation regions formed in said wafer,

said wafer being divided into a plurality of first portions, second portions, and third portions;

said first portions comprise gate dielectric capacitors, said gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer; wherein the first electrode layer is formed from said active layer, the insulating layer is formed from said gate dielectric layer, and the second electrode layer is formed from said conductive layer;

said second portions comprise first dummy structures, said first dummy structures comprise a first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from said active layer and the insulating layer of the first dummy structures is formed from said gate dielectric layer, wherein said second portion does not contain said conductive layer; and

said third portions comprise second dummy structures, said second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from said conductive layer, wherein said third portion does not contain said active

layer.

2. The wafer of claim 1, wherein the isolation regions are shallow trench isolation regions.

3. The wafer of claim 1, wherein said conductive layer comprises polysilicon.

4. The wafer of claim 1, wherein said active layer comprises doped silicon.

5. The wafer of claim 1, further comprising an interconnect layer formed over said conductive layer.

6. The wafer of claim 5, wherein said interconnect layer comprises a metal.

8. The wafer of claim 1, further comprising a silicon electrode contacting an isolation region.

10. The wafer of claim 1, wherein said gate dielectric capacitor is a transistor.

21. A wafer comprising:

a base layer;

an active layer formed on the base layer;

a gate dielectric layer formed on the active layer;

a conductive layer formed on the gate dielectric layer; and

a plurality of isolation regions formed in said wafer,

said wafer being divided into a plurality of first portions, second portions, and third portions;

said first portions comprise gate dielectric capacitors, said gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer; wherein the first electrode layer is formed from said active layer, the insulating layer is formed from said gate dielectric layer, and the second electrode layer is formed from said conductive layer, wherein said active layer comprises source/drain regions;

said second portions comprise first dummy structures, said first dummy structures comprise a

first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from said active layer and the insulating layer of the first dummy structures is formed from said gate dielectric layer, wherein said second portion does not contain said conductive layer; and

said third portions comprise second dummy structures, said second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from said conductive layer, wherein said third portion does not contain said active layer.

22. The wafer of claim 8, wherein said silicon electrode is an electrically isolated polysilicon electrode that contacts an isolation region of the second dummy pattern.

23. A wafer comprising:

a base layer;

an active layer formed on the base layer;

a gate dielectric layer formed on the active layer;

a conductive layer formed on the gate dielectric layer; and

a plurality of isolation regions formed in said wafer,

said wafer being divided into a plurality of first portions, second portions, and third portions;

said first portions comprise gate dielectric capacitors, said gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer; wherein the first electrode layer is formed from said active layer, the insulating layer is formed from said gate dielectric layer, and the second electrode layer is formed from said conductive layer, wherein said gate dielectric layer is located between said first electrode layer and said second electrode layer;

said second portions comprise first dummy structures, said first dummy structures comprise a first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from said active layer and the insulating layer of the first dummy structures is formed from said gate dielectric layer, wherein said second portion does not contain said conductive layer; and

said third portions comprise second dummy structures, said second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from said conductive layer, wherein said third portion does not contain said active layer.

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consideration pursuant to a restriction requirement. Claims 1-6, 8, and 21-23 have been finally rejected. It is from the final rejection of claims 1-6, 8, and 21-23 that this appeal is taken.

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V. SUMMARY OF INVENTION

This invention addresses and solves the problem of accurately measuring the gate dielectric thickness and the capacitance of gate dielectric capacitors (page 2, lines 18 to 23 of the written description). This invention provides a wafer comprising a plurality of dummy structures that allows gate dielectric thickness and capacitance to be monitored and measured with improved accuracy before the wafer is cut into individual chips (page 6, lines 8 and 9 of the written description).

An important aim of ongoing research in the semiconductor industry is the reduction in the dimensions of semiconductor devices. As the size of planar transistors such as metal oxide semiconductor field effect transistors (MOSFET) devices decreases, the dimensions of the gate electrodes and gate dielectric layers decrease correspondingly. Tight control of the gate dielectric thickness is necessary to manufacture reduced-size, high-reliability, high-speed transistors. If the gate dielectric thickness is too thin, short-circuiting is a problem. If the gate dielectric layer is too thick, then the device speed will be too slow (page 1, lines 5 to 18 of the written description).

The thickness of the gate dielectric layer can be determined by measuring the capacitance of the

gate dielectric capacitor. The thickness of the gate dielectric layer is related to the capacitance by the following formula:

$$t = k/C$$

wherein t is the thickness of the gate dielectric layer, k is the dielectric constant of the gate dielectric layer, and C is the capacitance of the gate dielectric capacitor (page 1, lines 19 to 24 of the written description).

However, the capacitance of large area, ultra-thin gate dielectric capacitors and small area gate dielectric capacitors cannot be accurately measured directly. The large area gate dielectric capacitors tend to suffer from high gate leakage through the gate. Gate leakage does not appreciably hinder measuring the capacitance of small area gate dielectric capacitors, rather parasitic capacitance interferes with accurate gate dielectric capacitance measurements in small area gate dielectric capacitors. As the area of the gate dielectric capacitor is reduced, the proportion of the total capacitance due to the parasitic capacitance associated with the wiring structures increases (page 2, lines 1 to 8 of the written description).

Accurate measurement of the gate dielectric thickness and the capacitance of gate dielectric capacitors can be achieved with embodiments of the present invention, which provide a wafer comprising a base layer and an active layer formed on the base layer. A gate dielectric layer is formed on the active layer and a conductive layer is formed on the gate dielectric layer. A plurality of isolation regions are formed in the wafer and the wafer is divided into a plurality of first portions, second portions, and third portions. The first portions comprise gate dielectric capacitors, wherein the gate dielectric capacitors comprise a first electrode layer formed from the active layer, an insulating layer formed from the gate dielectric layer, and a second electrode layer formed from the conductive layer.

The second portions comprise first dummy structures, wherein the first dummy structures comprise a first electrode layer formed from the active layer and an insulating layer formed from the gate dielectric layer. The third portions comprise second dummy structures, wherein the second dummy structures comprise an insulating layer formed from an isolation region and a second electrode layer formed from the conductive layer. The third portion does not contain the active layer (page 2, line 23 to page 3, line 3; and page 15, lines 15 to 19 of the written description.)

This invention addresses the needs for an improved method of measuring the capacitance and gate dielectric thickness of ultra-thin gate dielectric capacitors. The present invention eliminates parasitic capacitance from the gate dielectric capacitance measurements enabling accurate measurement of the gate dielectric capacitor capacitance.

VI. ISSUES

A. The Rejection

Claims 1-6, 8, 10, and 21-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Admitted Prior Art (APA) (Figure 7) in view of Tuan et al. (U.S. Pat. App. 2002/0151141) and Baliga (U.S. Pat. App. 2002/0177277).

B. The Issues

The Issues that arise in this appeal that require resolution by the Honorable Board of Appeals and Interferences (the Board) are:

Whether claims 1-6, 8, 10, and 21-23 are unpatentable under 35 U.S.C. § 103(a) for obviousness as predicated upon the combination of APA, Tuan et al., and Baliga.

VII. GROUPING OF CLAIMS

There are three groups of claims. Claims 1-6, 8, 10, and 22 all stand or fall together. Claims 21 and 23 stand separately. Separate arguments in support of each group are presented *infra.*

VIII. THE ARGUMENT

A. The Examiner's Position

The Examiner asserted that Prior Art Figure 7 of the instant specification teaches a wafer comprising a base layer, gate dielectric layer, conductive layer, active region, a plurality of shallow isolation regions, and a metal interconnect. The Examiner acknowledged that the admitted prior art does not teach a wafer divided into a plurality of the claimed first, second, and third portions. The Examiner relied on Tuan et al. to provide a teaching of a wafer divided into first, second, and third portions, wherein the first portion comprises a gate electrode and the third portion comprises a second dummy structure. The Examiner further relied on Baliga to provide a teaching of the second portion (first dummy structure). The Examiner averred that the Tuan et al. dummy structures 141 correspond to the claimed second dummy structure and that the Baliga dummy structure 118c corresponds to the claimed first dummy structure. The Examiner concluded that it would have been obvious to modify the Admitted Prior Art gate structure to include the dummy structures of Tuan et al. and Baliga to provide a structure that can support high voltages.

B. Appellants' Position

The Admitted Prior Art, Tuan et al., and Baliga, whether taken alone, or in combination, do not suggest the claimed wafer. The Examiner proposed combination does not disclose or suggest the first

dummy structure. There is no motivation to include a selected portion of the Baliga structure in the Admitted Prior Art to obtain the device of claims 1, 21, and 23.

Claims 1, 21, and 23 require that the second portion does not contain the conductive layer. The Examiner asserted that the dummy structure 118c of Baliga comprises the first electrode layer and an insulating layer. The Examiner asserted that the doped silicon active layer of Baliga corresponds to the first electrode layer and that the insulating layer of Baliga corresponds to the gate dielectric layer.

The Examiner asserted that incorporating the second portions of Baliga into the APA would provide a structure that can support high voltages. However, the Examiner does not include the required conductive layers 118a, 118b, 118c of the Baliga structure when combining Baliga with the APA. Layers 118a, 118b, and 118c of Baliga are formed from the same layer and correspond to the conductive layer (second electrode layer) of a gate capacitor. The Examiner apparently ignored the Baliga conductive layers 118a, 118b, and 118c that are required components of the Baliga device. It is not seen how it is possible for the Examiner to allege motivation to only include a part of the asserted Baliga second portion in the APA. Presumably, the motivation asserted to be taught by Baliga would require the substitution of the entire asserted second portion. The entire asserted second portion of Baliga would include the conductive layers 118a, 118b, and 118c. However, claims 1, 21, and 23 explicitly exclude the presence of the conductive layers in the claimed second portions. Therefore, the combination of Baliga with Tuan et al. and the APA would not provide nor suggest the claimed wafer.

Claim 21 is further distinguishable because claim 21 requires that the active layer comprises source/drain regions. The Examiner asserted active layer 124 of Tuan et al. does not comprise source/drain regions. In addition, there is no motivation in Baliga to substitute source and drain regions into the first electrode layer 124 of Tuan et al.

Claim 23 is further distinguishable over the cited prior art because the cited prior art does not

suggest the claimed wafer wherein the gate dielectric layer is located between the first electrode layer and the second electrode layer. For example, the gate dielectric layer 108 of Tuan et al. is located beneath the Examiner asserted first and second electrode layers 124, 128, not between the electrode layers, as required by claim 23.

There is no suggestion in the cited references to combine Tuan et al., Baliga, and the APA as asserted by the Examiner to provide the claimed wafer.

The dummy gate structures of Tuan et al. protect circuit elements during chemical-mechanical polishing (CMP). The APA does not disclose performing CMP after forming circuit elements, as taught by Tuan et al. Therefore, there would be no suggestion to include the dummy structures of Tuan et al. in the wafer of the APA. Furthermore, Tuan et al. teach a high voltage portion 4402 of the semiconductor structure. Because the semiconductor structure of Tuan et al. already supports high voltage, there is no motivation to include the additional dummy structures of Baliga. One of ordinary skill in this art would not be motivated to include additional dummy structures to provide a structure that can support high voltages, when the structure already can support high voltages without the additional dummy structures.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge readily available to one of ordinary skill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). There is no suggestion in Tuan et al. or Baliga of substituting the claimed first and second dummy structures into the wafer of the Admitted Prior Art. There is no suggestion in Tuan et al. or Baliga of forming the claimed second portion in the wafer of the APA, as

required by claims 1, 21, and 23. There is no suggestion in Tuan et al. or Baliga to form the active layer comprising source/drain regions, as required by claim 21. In addition, there is no suggestion in Tuan et al. or Baliga to form the gate dielectric layer between the first and second electrode layers, as required by claim 23.

The mere fact that references can be modified does not render the resulting combination obvious unless the prior art also suggests the desirability of the modification. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Tuan et al. and Baliga do not suggest the desirability of forming the claimed first and second dummy structures and a gate dielectric capacitor on a wafer, as required by the instant claims.

The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103 is not an abstract concept, but must stem from the applied prior art as a whole and realistically impel one having ordinary skill in the art to modify a specific reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Accordingly, the Examiner is charged with the initial burden of identifying a source in the applied prior art for the requisite realistic motivation. *Smiths Industries Medical System v. Vital Signs, Inc.,* 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999); *In re Mayne*, 104 F.3d 1339, 41 USPQ2d 1449 (Fed. Cir. 1997). There is no motivation in Tuan et al. or Baliga to form a wafer comprising the claimed first and second dummy structures and a gate dielectric capacitor.

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The Examiner asserted that motivation for combining the references can be found in paragraph 013 of Tuan et al. However, no discernible motivation is found in Tuan et al. Perhaps, the Examiner intended to refer to paragraph 013 of Baliga. As explained above, it is not seen how Baliga can provide the asserted motivation when the Examiner selectively omits critical portions of the Baliga device from the asserted combination.

IX. CONCLUSION

Based upon the arguments submitted supra, Appellants respectfully submit that the Examiner's rejections under 35 U.S.C. § 103 are not legally viable. Appellants, therefore, respectfully solicit the Honorable Board to reverse the Examiner's rejections of claims 1-6, 8, 10, and 21-23 as obvious as evidenced by the APA, Tuan et al., and Bilaga.

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Respectfully submitted,

MCDERMOTT, WILL & EMERY

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Registration No. 46,429

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 BPC:rrh
Date: February 13, 2004
Facsimile: (202) 756-8087

X. APPENDIX

APPEALED CLAIMS:

1. A wafer comprising:

a base layer;

an active layer formed on the base layer;

a gate dielectric layer formed on the active layer;

a conductive layer formed on the gate dielectric layer; and

a plurality of isolation regions formed in said wafer,

said wafer being divided into a plurality of first portions, second portions, and third portions;

said first portions comprise gate dielectric capacitors, said gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer; wherein the first electrode layer is formed from said active layer, the insulating layer is formed from said gate dielectric layer, and the second electrode layer is formed from said conductive layer;

said second portions comprise first dummy structures, said first dummy structures comprise a first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from said active layer and the insulating layer of the first dummy structures is formed from said gate dielectric layer, wherein said second portion does not contain said conductive layer; and

said third portions comprise second dummy structures, said second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from said conductive layer, wherein said third portion does not contain said active

layer.

2. The wafer of claim 1, wherein the isolation regions are shallow trench isolation regions.

3. The wafer of claim 1, wherein said conductive layer comprises polysilicon.

4. The wafer of claim 1, wherein said active layer comprises doped silicon.

5. The wafer of claim 1, further comprising an interconnect layer formed over said conductive layer.

6. The wafer of claim 5, wherein said interconnect layer comprises a metal.

8. The wafer of claim 1, further comprising a silicon electrode contacting an isolation region.

10. The wafer of claim 1, wherein said gate dielectric capacitor is a transistor.

21. A wafer comprising:

a base layer;

an active layer formed on the base layer;

a gate dielectric layer formed on the active layer;

a conductive layer formed on the gate dielectric layer; and

a plurality of isolation regions formed in said wafer,

said wafer being divided into a plurality of first portions, second portions, and third portions;

said first portions comprise gate dielectric capacitors, said gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer; wherein the first electrode layer is formed from said active layer, the insulating layer is formed from said gate dielectric layer, and the second electrode layer is formed from said conductive layer, wherein said active layer comprises source/drain regions;

said second portions comprise first dummy structures, said first dummy structures comprise a

first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from said active layer and the insulating layer of the first dummy structures is formed from said gate dielectric layer, wherein said second portion does not contain said conductive layer; and

said third portions comprise second dummy structures, said second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from said conductive layer, wherein said third portion does not contain said active layer.

22. The wafer of claim 8, wherein said silicon electrode is an electrically isolated polysilicon electrode that contacts an isolation region of the second dummy pattern.

23. A wafer comprising:

a base layer;

an active layer formed on the base layer;

a gate dielectric layer formed on the active layer;

a conductive layer formed on the gate dielectric layer; and

a plurality of isolation regions formed in said wafer,

said wafer being divided into a plurality of first portions, second portions, and third portions;

said first portions comprise gate dielectric capacitors, said gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer; wherein the first electrode layer is formed from said active layer, the insulating layer is formed from said gate dielectric layer, and the second electrode layer is formed from said conductive layer, wherein said gate dielectric layer is located between said first electrode layer and said second electrode layer;

said second portions comprise first dummy structures, said first dummy structures comprise a first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from said active layer and the insulating layer of the first dummy structures is formed from said gate dielectric layer, wherein said second portion does not contain said conductive layer; and

said third portions comprise second dummy structures, said second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from said conductive layer, wherein said third portion does not contain said active layer.